NYE08-10B6ST1G

Protected Triac

Silicon Bidirectional Thyristor

Designed for use in solid state relays, MPU interface, TTL logic and other light industrial or consumer applications. Supplied in surface mount package for use in automated manufacturing.

Features

- Sensitive Gate Trigger Current in Two Quadrants
- Blocking Voltage to 600 V
- Surface Mount Package
- Compliant with IEC6100−4−5
- These are Pb−Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (Sine Wave, 50 to 60 Hz, Gate Open, T_J = 25 to 125°C)	V_{DRM}, V_{RRM}	600	V
On−State Current RMS (T_C = 80°C) (Full Sine Wave 50 to 60 Hz)	$I_{T(RMS)}$	0.8	A
Peak Non−repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_C = 25°C)	I_{TSM}	8.0	A
Circuit Fusing Considerations (Pulse Width = 8.3 ms)	I^2t	0.4	A^2s
Peak Gate Power (T_C = 80°C, Pulse Width ≤ 1.0 μs)	P_{GM}	5.0	W
Average Gate Power (T_C = 80°C, t = 8.3 ms)	$P_{G(AV)}$	0.1	W
Non−Repetitive Line Peak Voltage (IEC6100−4−5)	V_{PP}	2.0	kV
Critical Rate of Rise of All−State Current (I_G = 2 x I_{GT}, t_r < 100 μs, T_J = 1255C)	di/dt	100	A/μs
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

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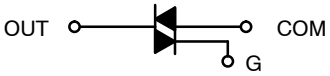
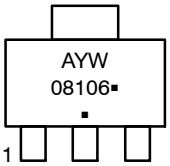
PROTECTED TRIAC
0.8 AMPERE RMS
600 VOLTS



SOT−223
CASE 318E

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
08106 = Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT	
1	OUT
2	COM
3	Gate
4	COM

ORDERING INFORMATION

Device	Package	Shipping†
NYE08−10B6ST1G	SOT−223 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

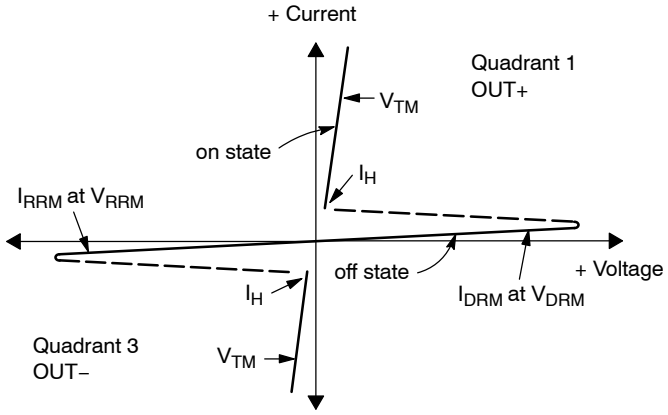
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	50	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	160	°C/W
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

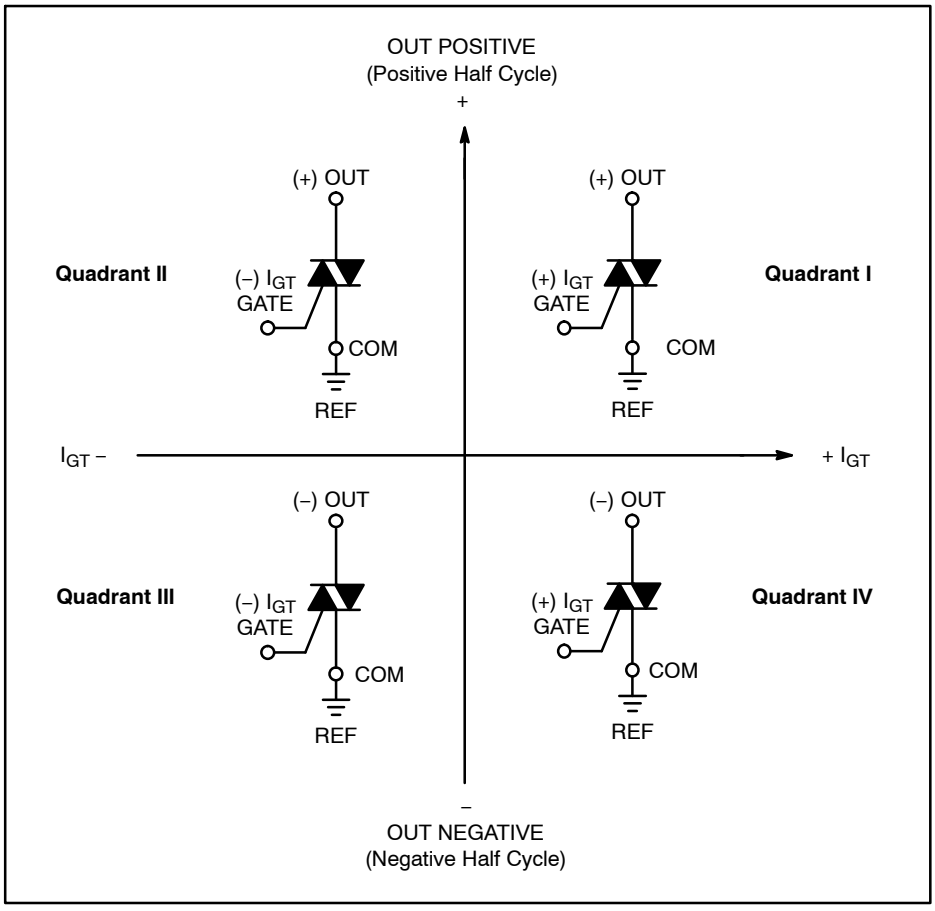
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Blocking Current	T_J = 25°C	I_{DRM}, I_{RRM}	−	−	2.0	μA
(V_D = V_{DRM}/V_{RRM}; Gate Open)	T_J = +125°C		−	−	200	μA
ON CHARACTERISTICS						
Peak On−State Voltage (I_{TM} = ±1.1 A Peak; Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2.0%)		V_{TM}	−	−	1.3	V
Gate Trigger Current (dc) (V_D = 12 Vdc, R_L = 30 Ω)		I_{GT}				mA
OUT(+), G(−)			0.15	−	10	
OUT(−), G(−)			0.15	−	10	
Latching Current (V_D = 12 V, I_G = 1.2 x I_{GT})		I_L				mA
OUT(+), G(−) All Types			−	−	30	
OUT(−), G(−) All Types			−	−	30	
Gate Trigger Voltage (dc) (V_D = 12 Vdc, R_L = 30 Ω)		V_{GT}	−	−	1.0	V
Gate Non−Trigger Voltage (V_D = 12 V, R_L = 30 Ω, T_J = 125°C) Quadrants 2, 3		V_{GD}	0.15	−	−	V
Dynamic Resistance		R_D	−	−	300	mΩ
Holding Current (V_D = 12 Vdc, Initiating Current = 50 mA, Gate Open)		I_H	−	−	25	mA
DYNAMIC CHARACTERISTICS						
Rate of Change of Commutating Current (Commutating dv/dt = 15 V/μs, Gate Open, T_J = 125°C, f = 250 Hz, without Snubber)		di/dt(c)	0.3	−	−	A/ms
Critical Rate of Rise of Off−State Voltage (V_D = 67% V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)		dv/dt	500	−	−	V/μs
Clamping Voltage (I_{CL} = 1.0 mA, t_p = 1 ms, T_J = 125°C)		V_{CL}	650	−	−	V

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to COM.

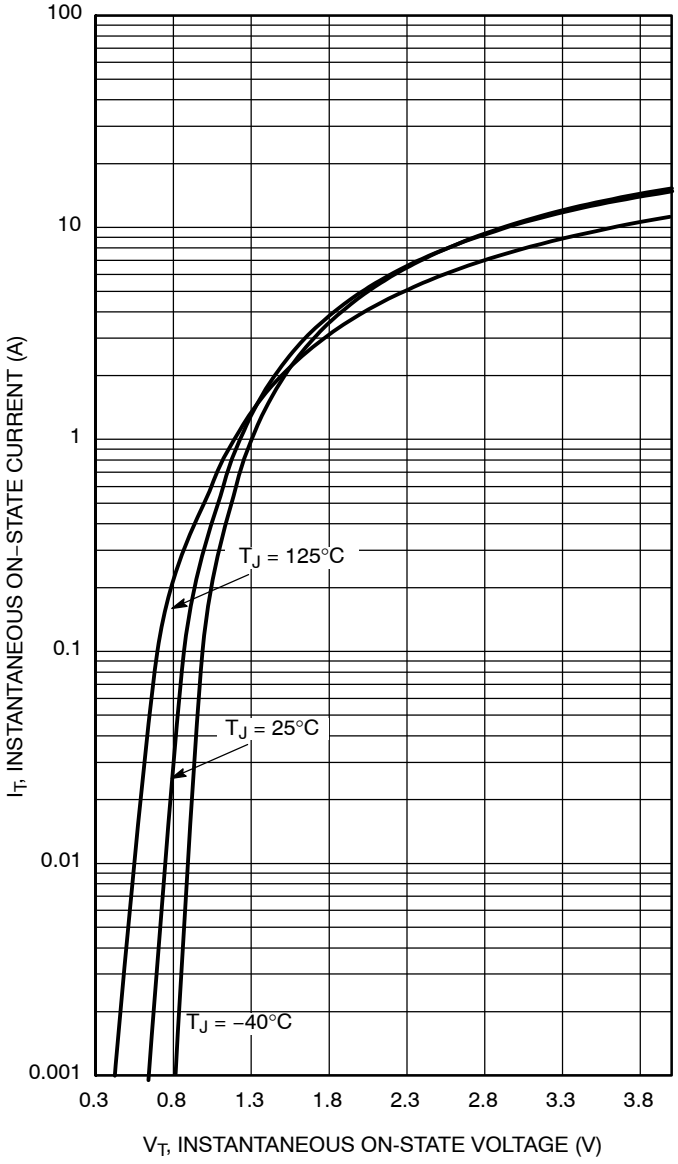


Figure 1. Maximum On−State Voltage Characteristics

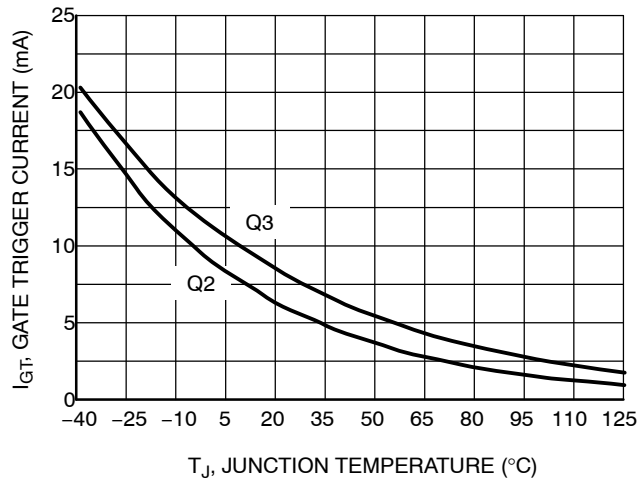


Figure 2. Typical Gate Trigger Current

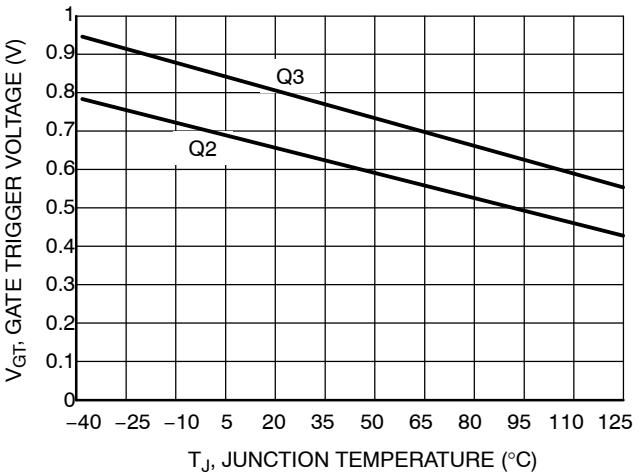


Figure 3. Typical Gate Trigger Voltage

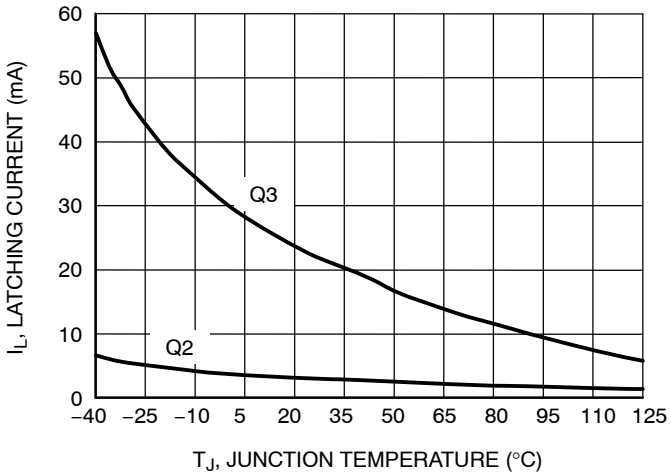


Figure 4. Typical Latching Current

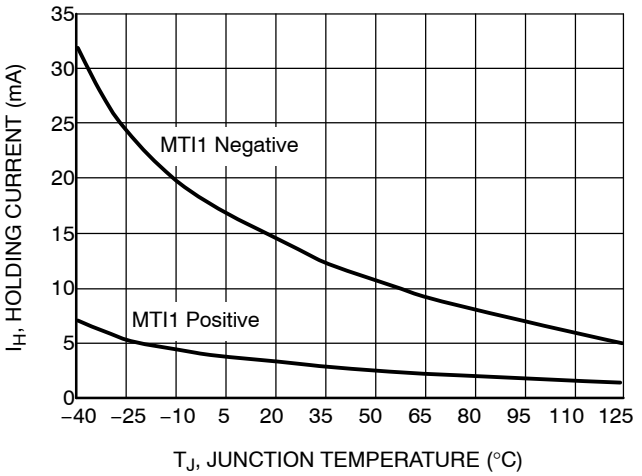
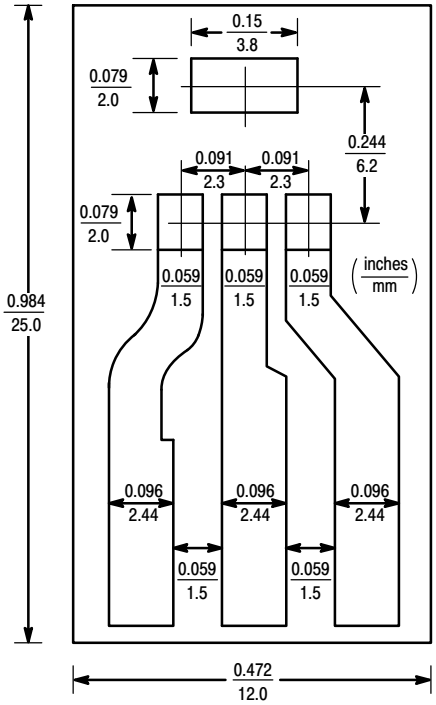


Figure 5. Typical Holding Current

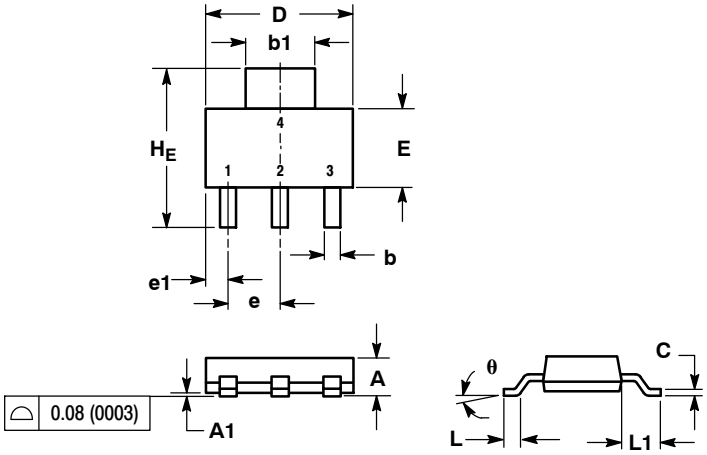


BOARD MOUNTED VERTICALLY IN CINCH 8840 EDGE CONNECTOR.
BOARD THICKNESS = 65 MIL., FOIL THICKNESS = 2.5 MIL.
MATERIAL: G10 FIBERGLASS BASE EPOXY

Figure 1. PCB for Thermal Impedance and Power Testing of SOT-223

PACKAGE DIMENSIONS

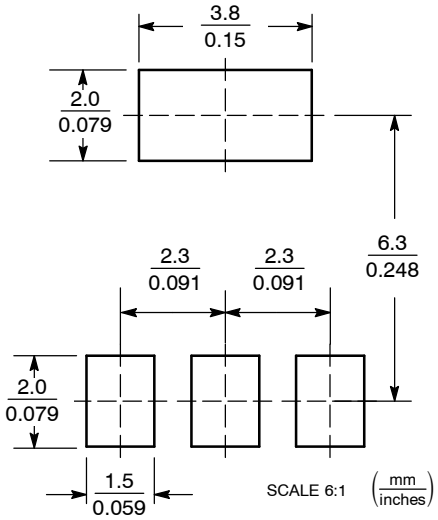
SOT−223 (TO−261)
CASE 318E−04
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	−−−	−−−	0.008	−−−	−−−
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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